

## TPD4E002 Quad Low-Capacitance Array with $\pm 15$ -kV ESD Protection

### 1 Features

- IEC 61000-4-2 ESD Protection
  - $\pm 15$ -kV IEC 61000-4-2 Contact Discharge
- IEC 61000-4-5 Surge Protection
  - 2.5-A Peak Pulse Current (8/20- $\mu$ s Pulse)
- ANSI/ESDA/JEDEC JS-001
  - $\pm 15$ -kV Human Body Model (HBM)
- Four Unidirectional Voltage Suppression Diodes for use in ESD Protection
- I/O Breakdown Voltage,  $V_{BR} = 6.1$  V (Minimum)
- I/O Capacitance 11 pF (Typical)
- Low Leakage Current  $< 100$  nA
- Very Small Printed-Circuit Board (PCB) Area  $< 2.6$  mm<sup>2</sup>
- High Integration
- Suitable for High-Density Boards

### 2 Applications

- Computers
- Printers
- Communication Systems and Cellular Phones
- Video Equipment

### 3 Description

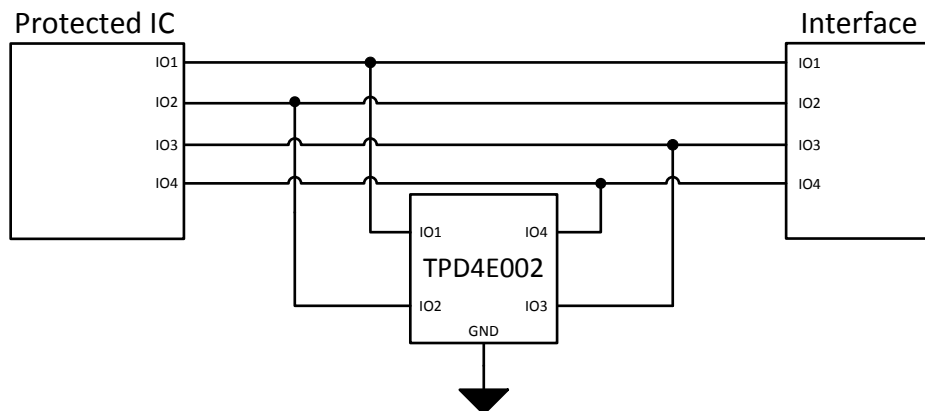
The TPD4E002 device is a transient voltage suppressor (TVS) designed to protect up to four lines against electrostatic discharge (ESD) transients. The monolithic circuit design allows superior capacitance matching between the channels and reduced crosstalk. This device is ideal for applications where both reduced line capacitance and board space-saving are required.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E002	SOT (5)	1.60 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Application Schematic



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Revision History</b> ..... 2 <b>5 Pin Configuration and Functions</b> ..... 3 <b>6 Specifications</b> ..... 4 6.1 Absolute Maximum Ratings ..... 4 6.2 ESD Ratings—JEDEC Specification..... 4 6.3 ESD Ratings—IEC Specification ..... 4 6.4 Recommended Operating Conditions ..... 4 6.5 Thermal Information ..... 4 6.6 Electrical Characteristics..... 5 6.7 Typical Characteristics ..... 6 <b>7 Detailed Description</b> ..... 7 7.1 Overview ..... 7 7.2 Functional Block Diagram ..... 7 7.3 Feature Description..... 7	7.4 Device Functional Modes..... 7 <b>8 Application and Implementation</b> ..... 8 8.1 Application Information..... 8 8.2 Typical Application ..... 8 <b>9 Power Supply Recommendations</b> ..... 9 <b>10 Layout</b> ..... 10 10.1 Layout Guidelines ..... 10 10.2 Layout Example ..... 10 <b>11 Device and Documentation Support</b> ..... 11 11.1 Documentation Support ..... 11 11.2 Receiving Notification of Documentation Updates 11 11.3 Community Resources..... 11 11.4 Trademarks ..... 11 11.5 Electrostatic Discharge Caution..... 11 11.6 Glossary ..... 11 <b>12 Mechanical, Packaging, and Orderable Information</b> ..... 11
---	---

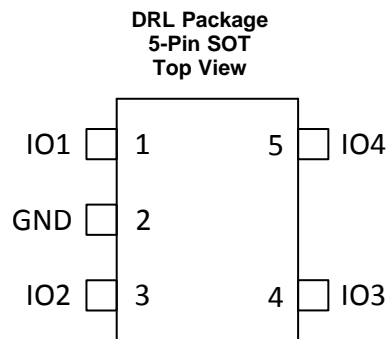
### 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2016) to Revision F	Page
• Updated the <i>Pin Functions</i> table .....	3

Changes from Revision D (July 2010) to Revision E	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Deleted Ordering Information table. See POA at the end of the document .....	1

## 5 Pin Configuration and Functions



PIN		TYPE	DESCRIPTION
NO.	NAME		
1	I/O1	I/O	ESD protection channel
2	GND	—	Ground
3	I/O2	I/O	ESD protection channel
4	I/O3	I/O	ESD protection channel
5	I/O4	I/O	ESD protection channel

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
T <sub>J</sub>	Junction temperature		125	°C
T <sub>op</sub>	Operating temperature	-40	125	°C
T <sub>stg</sub>	Storage temperature	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings—JEDEC Specification

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 contact discharge	±15000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>		
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
I <sub>pp</sub>	Peak pulse current	IEC 61000-4-5 (tp = 8/20 μs)	2.5	A
P <sub>pp</sub>	Peak pulse power	IEC 61000-4-5 (tp = 8/20 μs)	25	W

### 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>I/O</sub>	Operating voltage	0	5	V
	Operating temperature	-40	125	°C

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TPD4E002	UNIT	
	DRL (SOT)		
	5 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	220	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	80.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	42.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	42.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

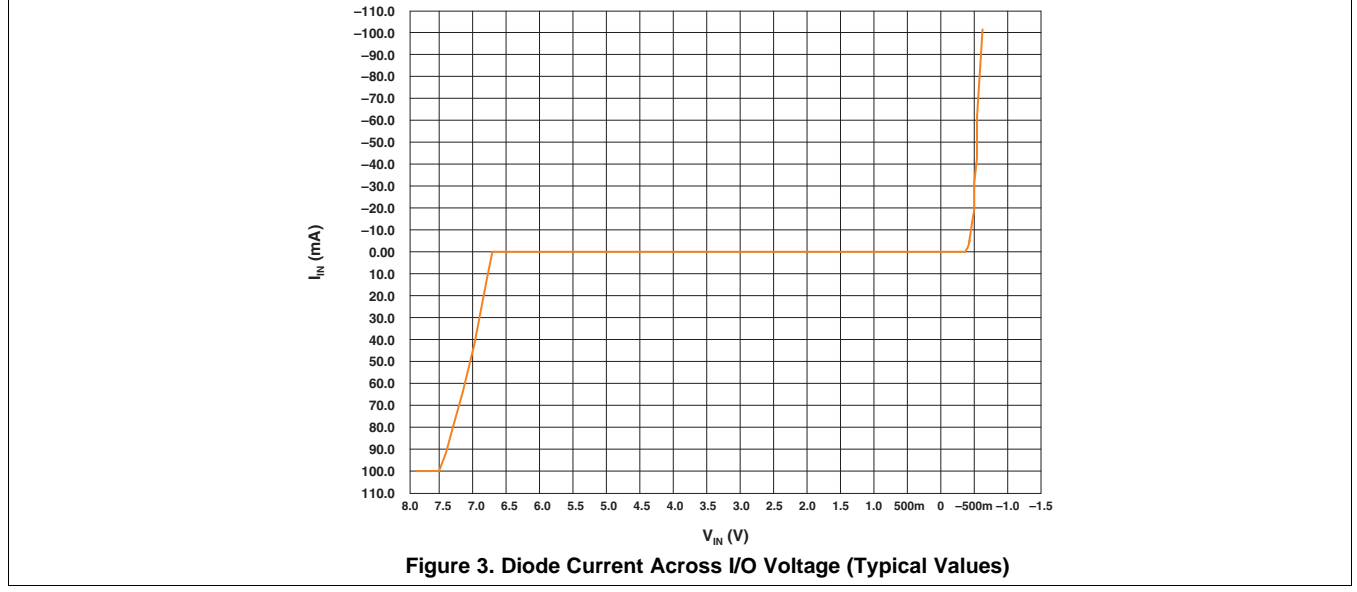
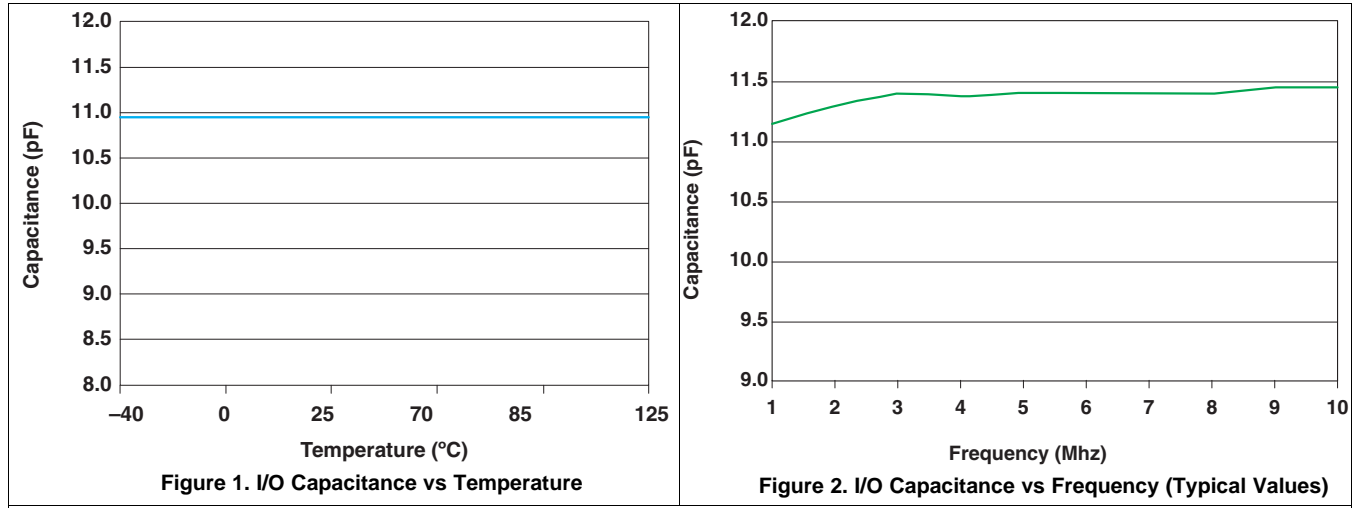
## 6.6 Electrical Characteristics

 $T_{amb} = 25^{\circ}\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BR}$	I/O breakdown voltage	$I_R = 1 \text{ mA}$	6.1		7.2	V
$I_{RM}$	I/O leakage current	$V_{RM} = 3 \text{ V}$			0.1	$\mu\text{A}$
$\alpha T$	Voltage temperature coefficient			4.5		$\text{mV}/^{\circ}\text{C}$
C	I/O capacitance per line			11		$\text{pF}$
$R_d$	Dynamic resistance <sup>(1)</sup>			2		$\Omega$

(1)  $R_d$  is measured under reverse breakdown condition with inrush current in the range of 1 A using pulse techniques.

### 6.7 Typical Characteristics

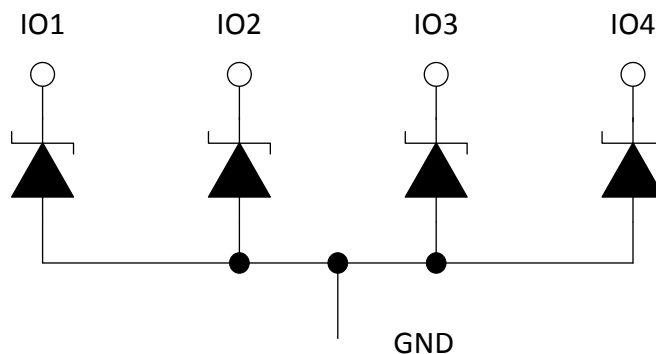


## 7 Detailed Description

### 7.1 Overview

The TPD4E002 is a four-channel TVS protection diode array. The TPD4E002 is rated to dissipate contact ESD strikes of  $\pm 15$  kV, beyond Level 4 as specified in the IEC 61000-4-2 international standard. This device has an 11-pF I/O capacitance per channel, making it ideal for use in data I/O interfaces of up to 100 MHz.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The TPD4E002 is a TVS that provides ESD protection for up to four channels, withstanding up to  $\pm 15$ -kV contact ESD per IEC 61000-4-2 and 2.5-A peak pulse current per IEC 61000-4-5. The monolithic technology yields exceptionally small variations in capacitance between any I/O pin of the TPD4E002. The small footprint is ideal for applications where space-saving designs are important.

### 7.4 Device Functional Modes

The TPD4E002 device is a passive integrated circuit that triggers when voltages are above  $V_{BR}$  or below the diodes  $V_F$  of approximately  $-0.5$  V. During ESD events, voltages as high as  $\pm 15$ -kV contact ESD can be directed to ground through the internal diodes. Once the voltages on the protected line fall below the trigger levels of TPD4E002 (usually within tens of nano seconds) the device reverts to its high-impedance state.

## 8 Application and Implementation

### NOTE

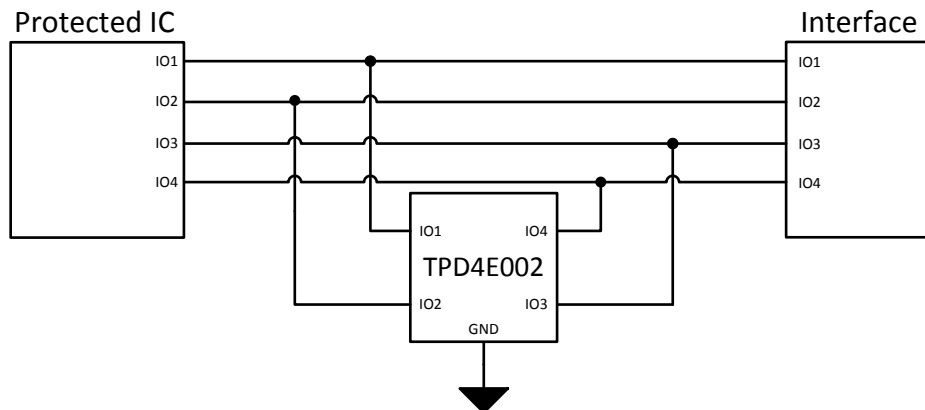
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPD4E002 device is a TVS diode array typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected integrated circuit (IC). The triggered TVS holds this voltage,  $V_{CLAMP}$ , to a safe level for the protected IC.

### 8.2 Typical Application

In a typical design example, one TPD4E002 device is being used to protect an IC against potential ESD from a four-channel human interface port, as shown in [Figure 4](#).



**Figure 4. Typical Application for TPD4E002**

#### 8.2.1 Design Requirements

[Table 1](#) lists the parameters for this typical application.

**Table 1. Design Parameters**

DESIGN PARAMETER	VALUE
Signal's voltage range on I/O1, I/O2, I/O3, and I/O4	0 V to 5 V
Operating frequency	< 100 MHz

#### 8.2.2 Detailed Design Procedure

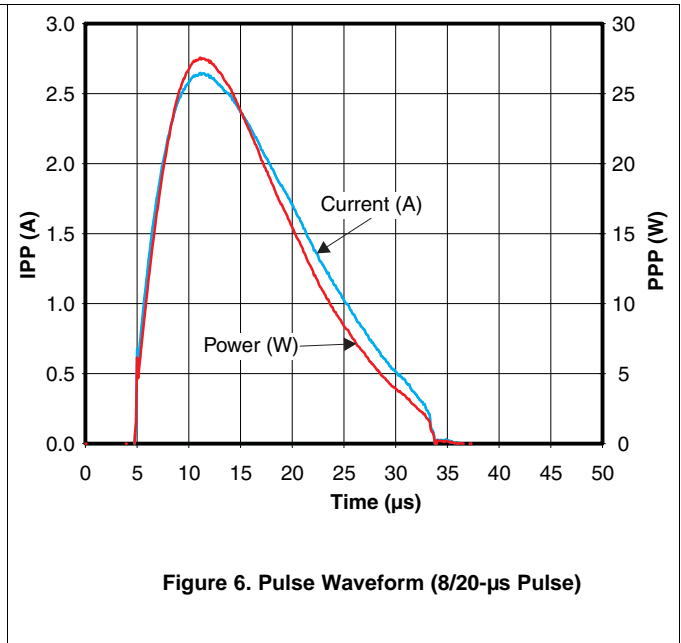
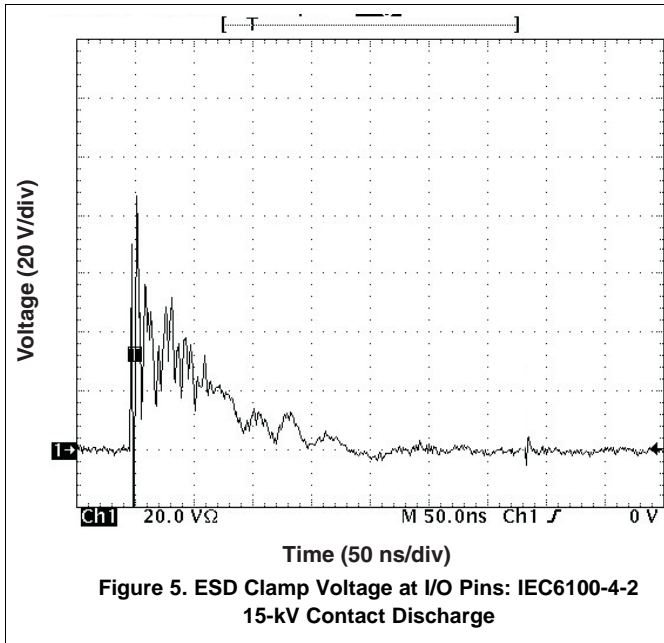
To begin the design process, some parameters must be decided upon; the designer must know the following:

- Voltage range of the signal on all protected lines
- Operating frequency on all protected lines

##### 8.2.2.1 Signal Range on I/O1 Through I/O2

The TPD4E002 device has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the four I/O channels will protect which signal lines. Any I/O supports a signal range of 0 V to 5 V and up to 100 MHz.

### 8.2.3 Application Curves



## 9 Power Supply Recommendations

The TPD4E002 is a passive ESD protection device and there is no need to power it. Do not violate the maximum voltage specifications for each pin.

## 10 Layout




### 10.1 Layout Guidelines

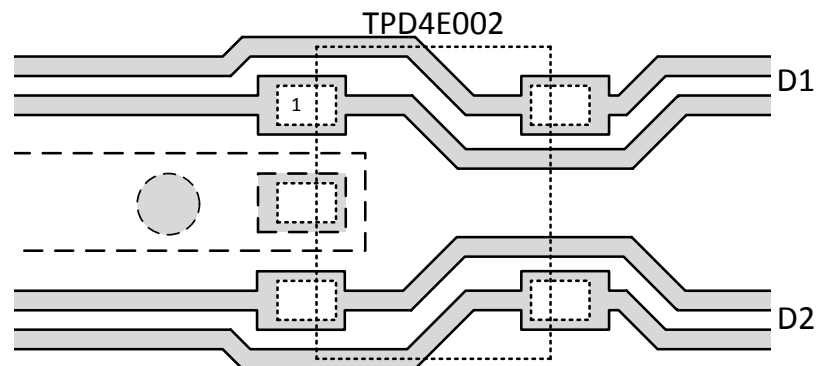
- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces, which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

Use external and internal ground planes and stitch them together with VIAs as close to the GND pin of TPD4E002 as possible. This allows for a low impedance path to ground so that the device can properly dissipate an ESD event.

### 10.2 Layout Example

#### Legend

-  VIA to Internal GND Plane
-  Pin to GND
-  Top Layer GND Plane



**Figure 7. TPD4E002 Example Layout**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- [Reading and Understanding an ESD Protection Datasheet](#)
- [ESD Layout Guide](#)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E002DRL2	ACTIVE	SOT-OTHER	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	28S	<a href="#">Samples</a>
TPD4E002DRLR	ACTIVE	SOT-OTHER	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	28S	<a href="#">Samples</a>
TPD4E002DRLRG4	ACTIVE	SOT-OTHER	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	28S	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

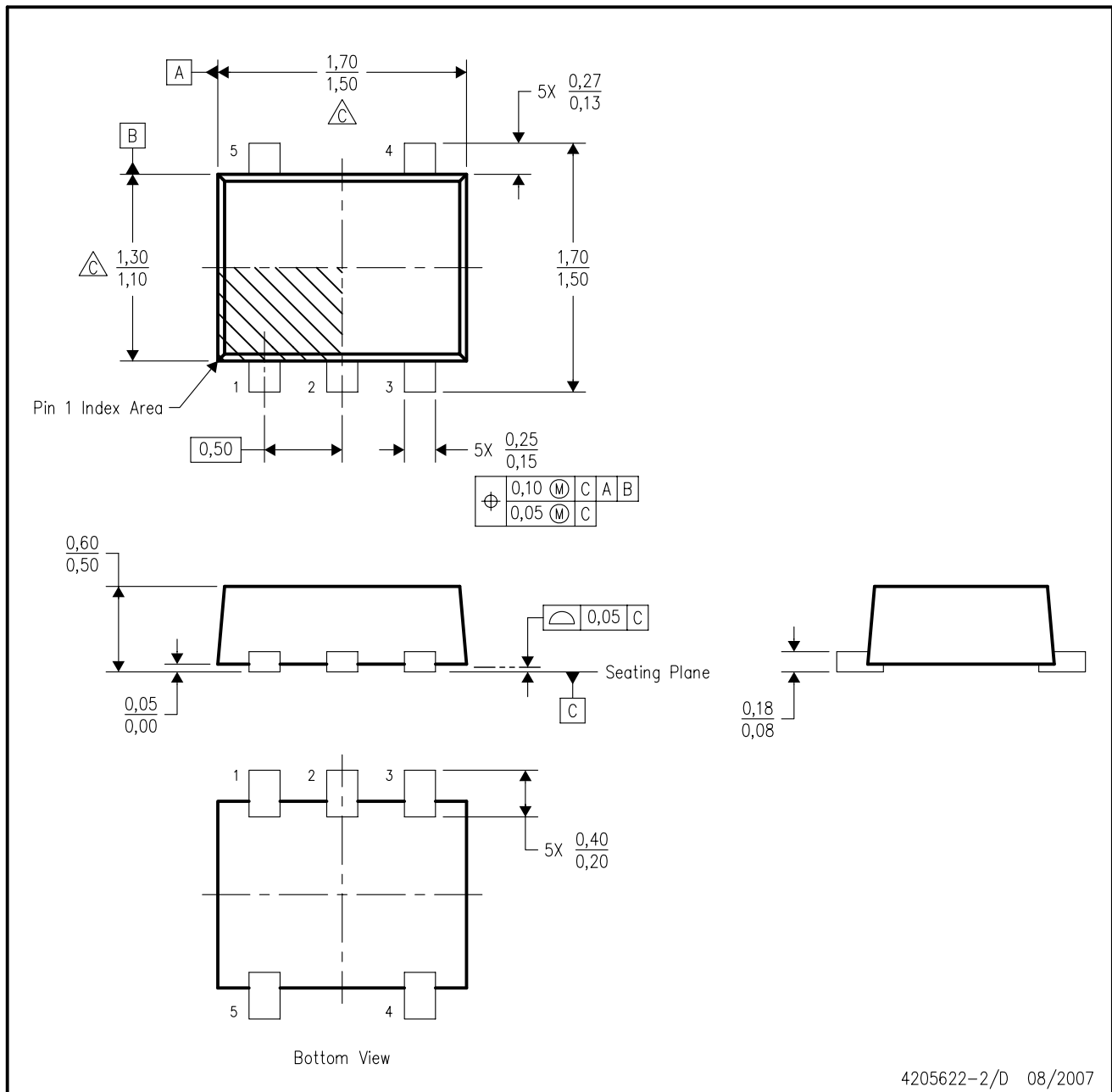

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E002DRL2	SOT-OTHER	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q2
TPD4E002DRLR	SOT-OTHER	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E002DRL2	SOT-OTHER	DRL	5	4000	202.0	201.0	28.0
TPD4E002DRLR	SOT-OTHER	DRL	5	4000	202.0	201.0	28.0

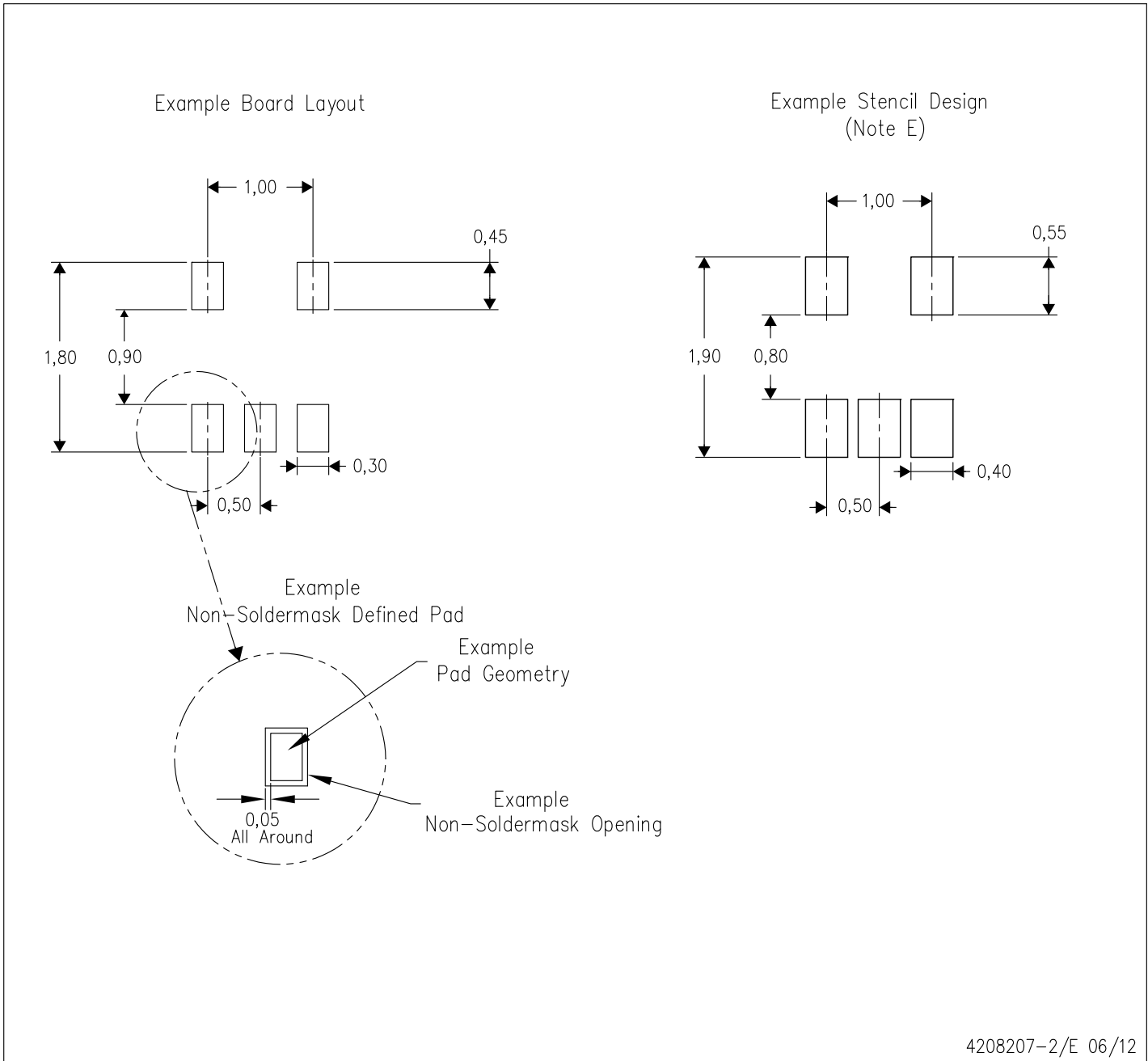


4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
  - D. JEDEC package registration is pending.

DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

## IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2017, Texas Instruments Incorporated